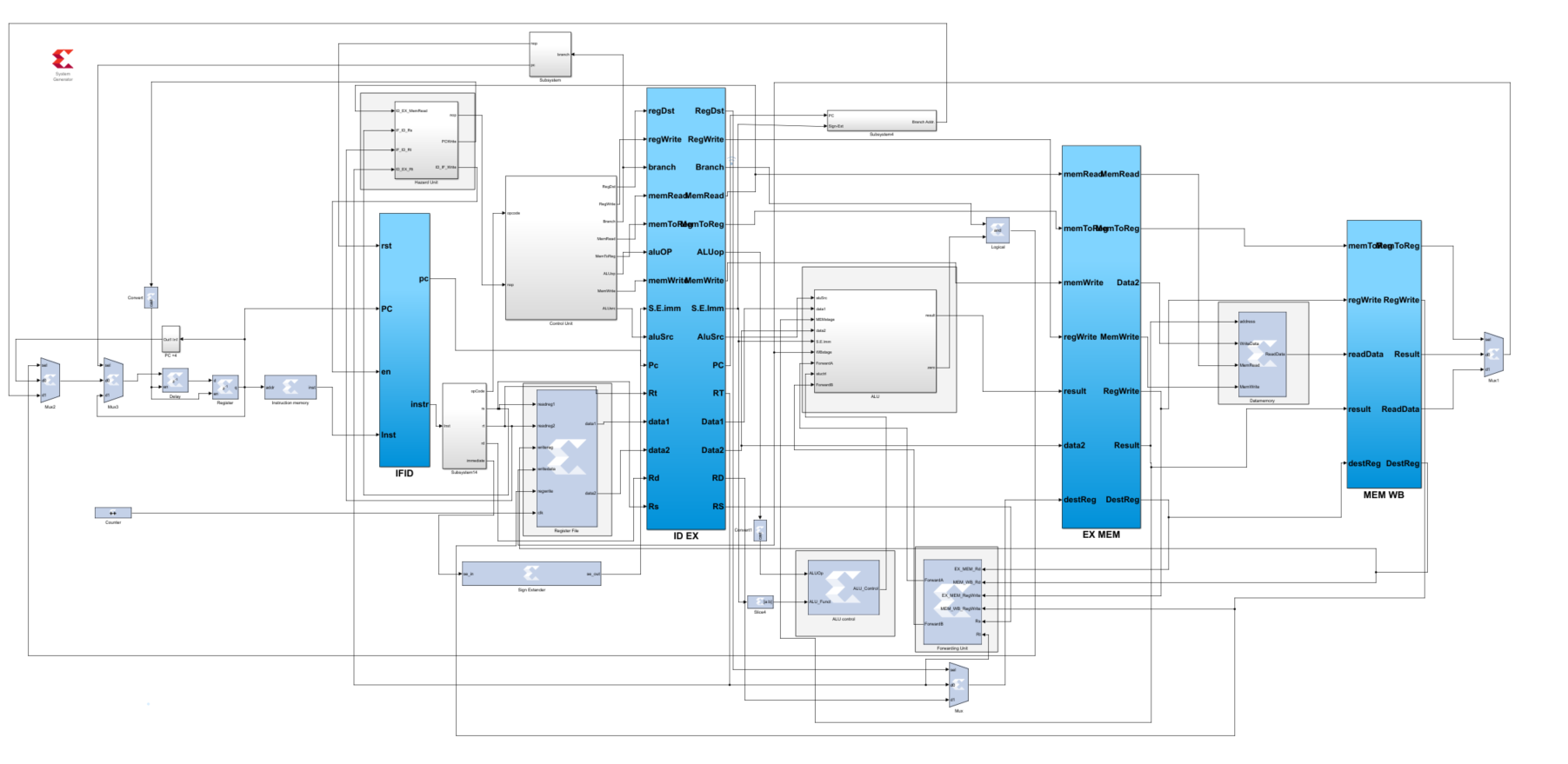
**ECTE 432 Computer Architecture Pipeline Project**

The Simulink model shown below was used to simulate the MIPS Pipeline Architecture

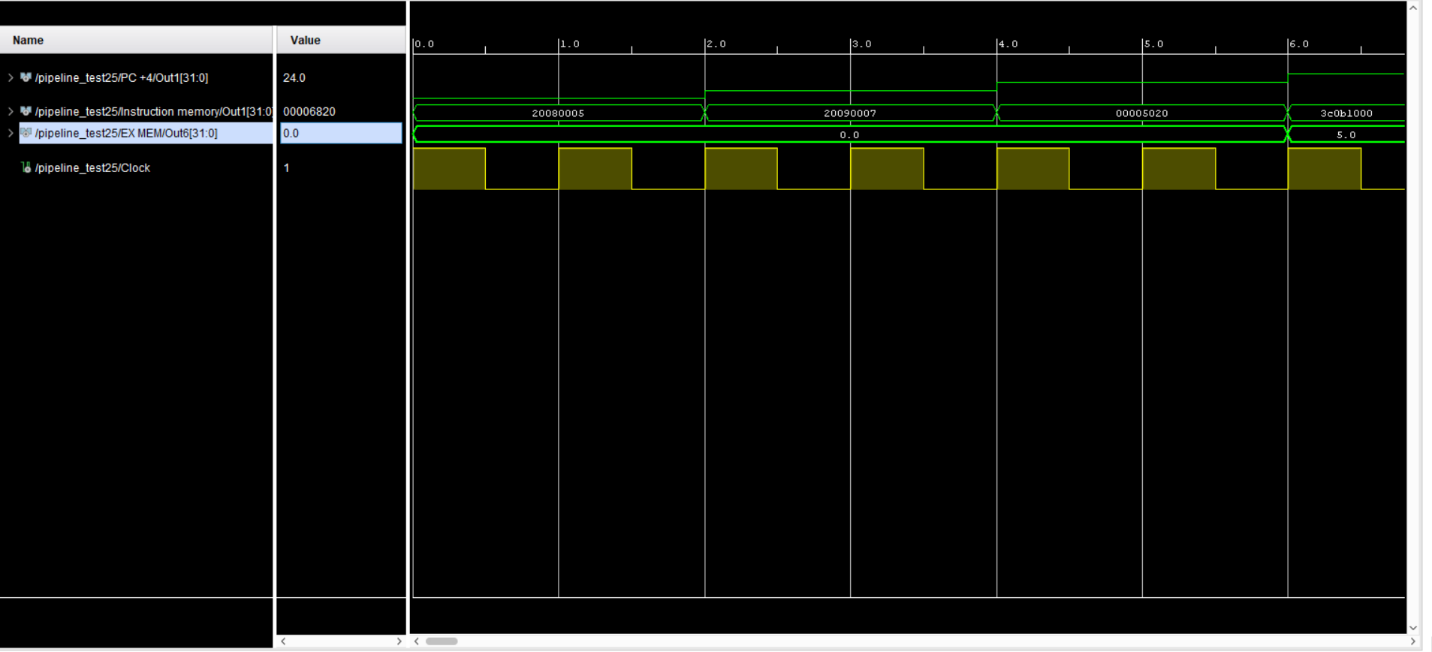


Some of the blocks were created in the Vivado using the VHDL file codes where as others were directly implemented using different in-built functions provided from the Xilinx Blockset.

The blocks of the following were created using Vivado :- Instruction Memory, Hazard Unit, Control Unit, Register Files, Control Unit, ALU, Forwarding Unit, Data memory & Sign Extender.

* PC : Counter setup that is incremented by 4 at every clock cycle.
* Control Unit: Control Unit is responsible for sending control signals for other blocks , this is done by decoding the opcode it receives as the input.
* Instruction memory : Stores the Hexadecimal values of test program.
* Hazard Unit: This block is coded when ever there is hazard detected while running the code
* ALU : The ALU stores the address of the data in the system.
* ALU control : Decodes r type functions and the functions performed by the ALU are controlled by the ALU control.
* Sign Extender : Converts 16-bit numbers to 32 bits if the msb of the immediate is 1 and append 16 ones in the beginning else append zeros.

**Output Results**



Four Outputs were displayed on the WaveForm viewer these are mainly the Program Counter Value, Clock, Result, Instruction Memory.

Some errors were displayed on the Waveform Viewer due to some errors in the Simulink model or the codes. The simulation are only 70-80% accurate since it produces wrong output data from the results.

